

An iterative merging placement algorithm for the fixed-outline floorplanning

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Abstract—Given a set of rectangular modules with fixed area and variable dimensions, and a fixed rectangular circuit. The placement of Fixed-Outline Floorplanning with Soft Modules (FOFSM) aims to determine the dimensions and position of each module on the circuit. We present a two-stage Iterative Merging Placement (IMP) algorithm for the FOFSM with zero deadspace constraint. The first stage iteratively merges two modules with the least area into a composite module to achieve a final composite module, and builds up a slicing tree in a bottom-up hierarchy. The second stage recursively determines the relative relationship (left-right or top-bottom) of the sibling modules in the slicing tree in a top-down hierarchy, and the dimensions and position of each leaf module are determined automatically. Compared with zero-dead-space (ZDS) algorithm, the only algorithm guarantees a feasible layout under some condition, we prove that the proposed IMP could construct a feasible layout under a more relaxed condition. Besides, IMP is more scalable in handling FOFSM considering the wirelength or without the zero deadspace constraint.

Index Terms—Placement, Floorplanning, Fixed-outline, Soft Modules, Zero Deadspace

I. INTRODUCTION

Floorplanning is a critical phase in the physical design of VLSI circuit. Nowadays, with the Integrated Circuit (IC) technology advance, design complexity is growing in a dramatic speed, and floorplanning remains to be a difficult problem. Given a set of rectangular modules and a netlist specifying the interconnection among the modules, the floorplanning asks to orthogonally place all the modules onto a rectangular circuit without overlapping, such that the area of the enveloping rectangle that exactly encloses all the modules and the total wirelength of the netlist are minimized. Under the wide utilization of the hierarchical methodology in the VLSI design [1], the outline of the circuit is usually specified beforehand, and the fixed-outline constraint has become a common feature for the floorplanning.

The modules in floorplanning can be classified into hard module and soft module. Hard module is in the fixed dimensions, while the soft module is in the fixed area but variable dimensions. Many algorithms have been developed in the past decades for the floorplanning with the two kinds of modules.

The most classic method to handle floorplanning with hard modules is to combine the representation of the geometric

relationships [2]–[5] among the modules with simulated annealing (SA) [6], [7]. In order to handle large scale modules, hierarchical and multilevel methodologies are adapted then. By scalably incorporating legalization into hierarchical flow, Cong et al. [8] proposed a partitioning to optimize module arrangement (PATOMA) algorithm, which utilized two placement algorithms zero-dead-space (ZDS) and row-oriented block (ROB) to guarantee the legalization of each partitioning. Based on the principle of Deferred Decision Making (DDM), Yan et al. [9] presented an efficient algorithm DeFer. Chan et al. [10] introduced a flexible flow to handle floorplanning with mixed modules, and there were two stages in their method: the global distribution stage aims to obtain shorter wirelength while distributing modules over the fixed-outline and the legalization stage aims to obtain feasible solution.

As the aspect ratio (the height divided by the width) of soft module varies continuously, the analytical method [11]–[15] is the most effective algorithm to handle floorplanning with soft modules. Luo et al. [11] introduced a nonlinear optimization methodology. First, it adapted a convex optimization to globally minimize the wirelength globally. Then, a further optimization and legalization was conducted by sizing the aspect ratio of the modules. Based on a recursive top-down area bipartitioning, Cong et al. [12] suggested a zero-dead-space (ZDS) placement algorithm for floorplanning with zero deadspace constraint. He et al. [13] and Lin et al. [14] proposed two representations, Ordered Quadtree and SKB-Tree, to encode the layout respectively. Given a topological structure, the above two methods could determine a corresponding layout by analytical approaches. Yan et al. [15] developed an optimal slack-driven block shaping (SDS) algorithm to shape the soft modules such that the resulting layout is inside the fixed outline.

In this paper, we present a two-stage Iterative Merging Placement (IMP) algorithm for the Fixed-Outline Floorplanning with Soft Modules (FOFSM) and zero deadspace constraint. At the first stage, all the modules are merged into one composite module by iteratively merging two modules with the least area. For each composite module generated in the first stage, the merging direction and relative position of

the two sub-modules have not specified. Then at the second stage, the final composite module is placed on the circuit, and the dimensions and positions of each pair of sub-modules are recursively determined basing on the aspect ratio of the composite module. We then present a mathematic analysis which shows IMP can place all the modules feasibly under some condition. Compared with ZDS, the only algorithm guarantees a feasible layout, the condition of IMP is more relaxed and IMP is more scalable in handling FOFSM considering the wirelength or having zero deadspace constraint.

The remainder of this paper is organized as follows. Section II presents the problem statement. Section III gives the definition of the composite module, and Section IV describes the Iterative Merging Placement (IMP) algorithm and analyzes conditions for feasible placement. The comparison between IMP and ZDS is discussed in Section V. And the paper is concluded in Section VI.

II. PROBLEM FORMULATION

Given a set of n soft modules with each module m_i has a fixed area s_i and an aspect ratio interval $[1/\lambda_i, \lambda_i]$ ($\lambda_i \geq 1$), and a fixed circuit with width W and height H . The placement of Fixed-Outline Floorplanning with Soft Modules (FOFSM) aims to determine the dimensions and position of each module on the circuit. Here λ_i is the bounding factor of m_i . Let (x_{i1}, y_{i1}) and (x_{i2}, y_{i2}) denote the coordinates of the bottom-left and upper-right vertices of m_i , let width w_i and height h_i represent the two dimensions of m_i . Then, the layout for the placement of FOFSM should satisfy the following constraints.

- (1) $x_{i2} - x_{i1} = w_i, y_{i2} - y_{i1} = h_i$
- (2) $1/\lambda_i \leq h_i/w_i \leq \lambda_i$
- (3) $\max(x_{i1} - x_{j2}, y_{i1} - y_{j2}, x_{j1} - x_{i2}, y_{j1} - y_{i2}) \geq 0$
- (4) $0 \leq x_{ik} \leq W, 0 \leq y_{ik} \leq H, k \in \{1, 2\}$

Here, i, j applies to $1, 2, \dots, n$ ($i \neq j$). Constraint (1) implies that each module should be placed orthogonally on the circuit; constraint (2) gives the aspect ratio interval of each module; constraint (3) indicates that all the modules should be placed with no overlapping and constraint (4) means all the modules should be completely placed on the circuit.

III. COMPOSITE MODULE

Similar to the composite pattern in software engineer, we define a conception of composite module in this section, and analyze its characters.

Definition 1 (composite module): A single soft module is a special composite module. Two composite modules could be merged horizontally or vertically to form a bigger composite module with their two pasted sides having the equal length, and the two modules are called the sub-modules of the bigger composite module.

Fig. 1 illustrates a composite module merged by m_1 and m_2 .

Definition 2 (feasible composite module): A composite module is a feasible composite module only if its aspect ratio interval covers $[1/\lambda, 1]$ or $[1, \lambda]$ ($\lambda \geq 1$) and its sub-modules

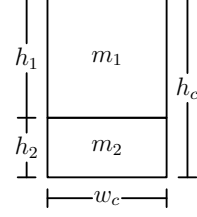


Fig. 1. composite module.

are feasible composite modules. And the two sub-modules can be merged feasibly.

Lemma 1: Two sub-modules, which can be merged into one feasible composite module having aspect ratio interval covers $[1/\lambda, 1]$ or $[1, \lambda]$, can construct any composite modules having aspect ratio is in $[1/\lambda, \lambda]$ feasibly.

Lemma 2: suppose there are two module m_1 and m_2 whose bounding factors are λ_1 and λ_2 respectively. Let $\alpha = s_1/s_2$ ($\alpha \geq 1$), if $1/(\lambda_1 - 1) \leq \alpha \leq \lambda_2 - 1$, then they can merge into a feasible composite module m_c whose bounding factor $\lambda_c \geq \min(\lambda_1, \lambda_2)$.

Proof: Without loss of generality, assume m_1 and m_2 are merged vertically, as shown in Fig. 1. Let h_i denotes the height of m_i , w_c and h_c represent the two dimensions of the composite module m_c . Since the bounding factors of m_1 and m_2 are λ_1 and λ_2 respectively

$$\frac{1}{\lambda_1} \leq \frac{h_1}{w} \leq \lambda_1, \frac{1}{\lambda_2} \leq \frac{h_2}{w} \leq \lambda_2$$

Thus

$$\max(\frac{1}{\lambda_1 h_1}, \frac{1}{\lambda_2 h_2}) \leq \frac{1}{w} \leq \min(\frac{\lambda_1}{h_1}, \frac{\lambda_2}{h_2})$$

Therefore

$$\max(\frac{h}{\lambda_1 h_1}, \frac{h}{\lambda_2 h_2}) \leq \frac{h}{w} \leq \min(\frac{\lambda_1 h}{h_1}, \frac{\lambda_2 h}{h_2})$$

As $s_1 = \alpha s_2$, $h_1 = \alpha h_2$ and $h = (1 + \alpha)h_2$. So, the aspect ratio interval of m_c is

$$\max(\frac{1 + \alpha}{\alpha \lambda_1}, \frac{1 + \alpha}{\lambda_2}) \leq \frac{h}{w} \leq \min[(1 + \frac{1}{\alpha})\lambda_1, (1 + \alpha)\lambda_2] \quad (1)$$

By Lemma 1, m_1 and m_2 can be merged feasibly if $[1, \lambda_c]$ is a subset of the aspect ratio interval of m_c . Thus the left part of (1) should be no greater than 1.

$$\max(\frac{1 + \alpha}{\alpha \lambda_1}, \frac{1 + \alpha}{\lambda_2}) \leq 1$$

so $1 + \alpha \leq \alpha \lambda_1$ and $1 + \alpha \leq \lambda_2$, and we get

$$\frac{1}{\lambda_1 - 1} \leq \alpha \leq \lambda_2 - 1 \quad (2)$$

the bounding factor of m_c :

Require: Module sequence m_1, m_2, \dots, m_n with respective areas $s_1 \geq s_2 \dots \geq s_n$;
Circuit region R of area $A = \sum_{k=1}^n s_k$ and dimensions $W \times H$;
Stage I
while current sequence contains more than one module **do**
 take out the two rearmost modules m_i and m_j in the sequence and merge them into a composite module m_c ;
 insert m_c in a position k of the sequence such that $s_{k-1} > s_k \geq s_{k+1}$;
 push m_c into stack S_T ;
end while
Stage II
place the only composite module in the sequence on the circuit;
while S_T is not null **do**
 pop one composite module m_c having two sub-modules m_i and m_j from stack S_T ;
 if $\gamma_c \geq 1$ **then**
 m_i and m_j merged vertically and the larger one is on the top;
 else
 m_i and m_j merged horizontally and the larger one is on the left;
 end if
 determining the aspect ratios and positions of m_i and m_j by Lemma 3;
end while

Fig. 2. The iterative merging placement (IMP) algorithm.

$$\lambda_c = \min[(1 + \frac{1}{\alpha})\lambda_1, (1 + \alpha)\lambda_2]$$

since $\alpha \geq 1$, $(1 + 1/\alpha)\lambda_1 \geq \lambda_1$ and $(1 + \alpha)\lambda_2 \geq \lambda_2$

$$\lambda_c \geq \min(\lambda_1, \lambda_2) \quad (3)$$

Lemma 3: Given the aspect ratio and the position of a composite module, if the merging direction and left-right/top-down order of the two sub-modules are specified, then the aspect ratios and positions of the two sub-modules can be determined uniquely.

As shown in Fig. 1, if we know m_1 and m_2 are merged vertically and m_1 is above m_2 . As the aspect ratio of the composite module is known, the value of w_c can be determined, and the two heights h_1 and h_2 can be determined then. The aspect ratios and positions of m_1 and m_2 are determined obviously.

IV. ITERATIVE MERGING PLACEMENT ALGORITHM

The Iterative Merging Placement (IMP) algorithm is a two-stage deterministic algorithm. At the first stage, by iteratively merging two modules with the least area, all the modules will finally be merged into one big composite module having the same area as the circuit. For each composite module generated in this stage, IMP just records its two sub-modules, while the merging direction and left-right/top-down order of the sub-modules are not specified. At second stage, first the final composite module is placed on the circuit such that its aspect ratio and position are specified. Then by Lemma 3, the aspect ratios and positions of each pair of sub-modules are determined based on the aspect ratio of the composite module recursively. The pseudo code of IMP is illustrated in Fig. 2.

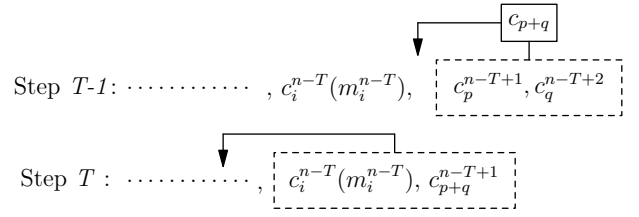


Fig. 3. The composite module c_{p+q} generated in step $T - 1$ insert at the rear of the sequence.

Lemma 4: The area of one composite module generated at step t of the IMP is no larger than the areas of any composite modules generated after step t .

At each step of stage I of the IMP, two modules with the least area are taken out to be merged into a composite module which will be inserted into the sequence then. Therefore, the two modules selected are not bigger than that in the following steps.

THEOREM 1: IMP can place all the modules feasibly under the following conditions,

- (1) all the modules have a uniform bounding factor λ ($\lambda \geq 3$).
- (2) the aspect ratio of the circuit γ_A is in the period $[1/\lambda, \lambda]$.
- (3) for all $i \in 1, 2, \dots, n - 1$,

$$\max \frac{s_i}{\sum_{j=i+1}^n s_j} \leq \lambda - 1$$

Proof: Since the bounding factors of all the given modules are λ , by Lemma 2 all the feasible composite modules generated in the IMP should have bounding factors no smaller than λ . Thus, to insure IMP can obtain a feasible layout, we just need to prove all the generated composite modules are feasible.

As $\lambda \geq 3$, the left side of the constraint $1/(\lambda_1 - 1) \leq \alpha \leq \lambda_2 - 1$ in Lemma 2 is always true. Thus, to insure m_1 and m_2 can merge feasibly, we just need to prove $\alpha \leq \lambda_2 - 1$.

Let c_i represents a composite module, c_i^j denotes that module c_i is located in position j in the current sequence. A mathematical induction is used here to prove the composite module generated at each step is feasible.

At step $T = 1$, m_{n-1} and m_n are going to be merged. According to condition (1) and (3), $s_{n-1}/s_n \leq \lambda - 1 = \lambda_n - 1$. Hence they can be merged feasibly.

Then we prove the following assertion: if all the composite modules generated at the first $T - 1$ steps are feasible. Then the sub-modules can be merged feasibly at step T :

If the composite module c_{p+q} generated at step $T - 1$ is inserted at the rear of the sequence, as shown in Fig. 3. By Lemma 4, c_i must be a single module, otherwise c_{p+q} would be inserted in front of c_i . Similarly, c_{p+q} is a composite module including $\{m_{i+1}, \dots, m_n\}$, otherwise there should be a step T_k ($1 \leq T_k < T - 1$) at which a subset of $\{m_{i+1}, \dots, m_n\}$ is merged into a composite module and inserted in front of c_i , and c_{p+q} should be inserted in front of c_i . Therefore

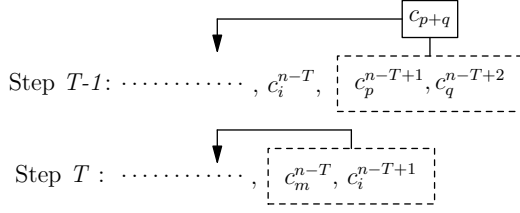


Fig. 4. The composite module c_{p+q} generated in step $T-1$ does not insert at the rear of the sequence.

$$\frac{s_i}{s_{p+q}} = \frac{s_i}{\sum_{j=i+1}^n s_j}$$

By the assertion c_{p+q} is a feasible composite module, $\lambda_{p+q} \geq \lambda$. Hence

$$\frac{s_i}{s_{p+q}} \leq \lambda - 1 \leq \lambda_{p+q} - 1$$

Otherwise, the composite module c_{p+q} generated at step $T-1$ is not inserted at the rear of the sequence, as shown in Fig. 4. As the sequence is organized in a non-increasing order, $s_i \geq s_p \geq s_q$, and, $s_{p+q} = s_p + s_q \leq 2s_i$. Because c_{p+q} is inserted in front of c_i , $s_m \leq s_{p+q}$. Therefore

$$\frac{s_m}{s_i} \leq \frac{s_{p+q}}{s_i} \leq 2 \leq \lambda_i - 1$$

Above all, the sub-modules can be merged feasibly at step T . ■

V. COMPARISON WITH ZDS

Based on a recursive top-down area bipartitioning, zero-dead-space (ZDS) [12] is an algorithm attempts to bound the aspect ratios of all the modules uniformly. At each step, the modules in a region are separated into two groups such that the total areas of the groups are as nearly equal as possible. The region is then cut parallel to its shorter side with each group fits exactly into one of the regions. Modules are placed once they fill a sufficient fraction of their subregions. To the best of our knowledge, ZDS is the only method that can deal with the placement of FOFSM under some condition. The condition is that all the given modules have a uniform upper bound λ ($\lambda \geq 3$), the aspect ratio of the circuit γ_A is in period $[1/\lambda, \lambda]$, and for all $i \in \{1, 2, \dots, n-1\}$, $\max(s_i/s_{i+1}) \leq \lambda - 1$.

IMP has a more relaxed condition to guarantee a feasible layout. As

$$\max\left(\frac{s_i}{\sum_{j=i+1}^n s_j}\right) \leq \max\left(\frac{s_i}{s_{i+1}}\right)$$

Furthermore, IMP is more scalable in handling a related problem, the placement of FOFSM without zero deadspace constraint. As a recursive top-down area bipartitioning method, there is a deadspace distribution at each step of ZDS. Therefore a backtracking to redistribute the deadspace is always necessary when ZDS fails to obtain a feasible layout. By comparison, IMP merges all the modules without the consideration of

deadspace distribution, and the aspect ratio intervals of all the composite modules generated in this process can be figured out, which can be used to guide the distributing deadspace to composite modules.

Also, IMP is more scalable in handling another related problem, the FOFSM and considering the wirelength. At each step, The merging operation of IMP is just to merge two modules, while the separating operation of ZDS is to separate a set of modules into two groups and partition the corresponding region. Therefore, the merging operation is simpler, which makes it easy to consider the wirelength optimization.

VI. CONCLUSION

In this paper, we deal with a continuous optimization problem, the placement of Fixed-Outline Floorplanning with Soft Modules (FOFSM), which aims to shape and place all the modules on a fixed circuit. Similar to the composite pattern in soft engineer, we proposed a conception of composite module. Based on this conception, an Iterative Merging Placement (IMP) algorithm is suggested to handle the placement of FOFSM. In the IMP, modules with the least area are prior to be merged, and after all the modules are merged, the dimensions and position of each module is determined recursively. We prove that IMP can obtain a feasible layout under a more relaxed condition. Moreover, it is more scalable in handling related problem that has deadspace or considering the wirelength.

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China (Grant no. 61173180 and 61272014).

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